SSC8021GN1

P-Channel Enhancement Mode MOSFET with ESD Protection

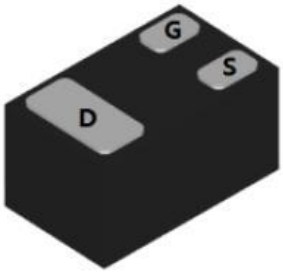
➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D	ESD
-20V	±12V	0.45Ω@-4V5	-1A	0.5kV
		0.6Ω@-2V5		

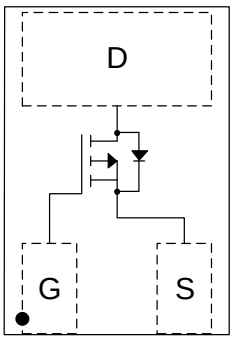
➢ Description

This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package. The product does not contain Rohs substances such as lead and halogen.

➢ Pin configuration



DFN1006-3L (Bottom View)



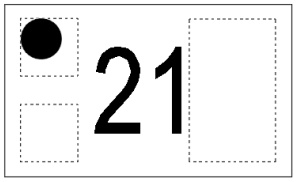
Pin Configuration (Top View)

● Applications

- Load Switch
- Portable Devices
- Signal Drive

➢ Ordering Information

Device	Package	Shipping
SSC8021GN1	DFN1006-3L	10000/Reel



Marking

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	±12	V
I_D	Continuous Drain Current [a]	-1	A
I_{DM}	Pulsed Drain Current [b]	-3	A
P_D	Power Dissipation [c]	0.45	W
P_{DSM}	Power Dissipation [a]	0.2	W
T_J	Operation junction temperature	-55~150	℃
T_{STG}	Storage temperature range	-55~150	℃

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	625	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	277	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

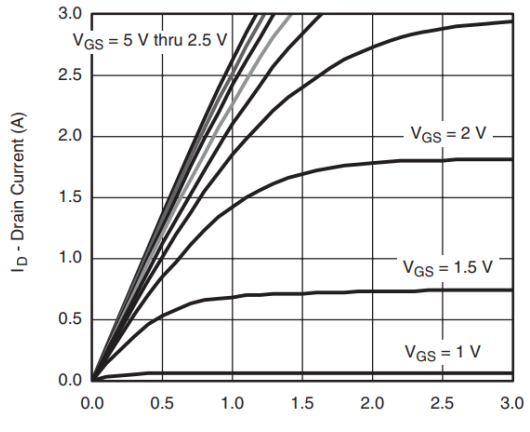
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

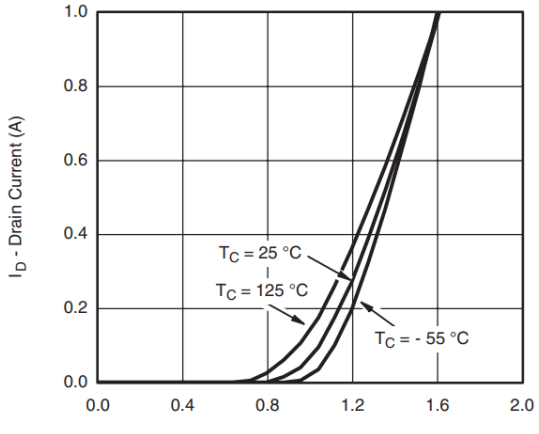
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250uA	-0.4	-0.7	-1	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -0.5A		450	650	mΩ
		V_{GS} = -2.5V, I_D = -0.3A		600	900	
		V_{GS} = -1.8V, I_D = -0.1A		800	1500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	μA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0V			±10	μA
Transconductance	G_{FS}	V_{DS} = -5V, I_D = -0.5A		1		s
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = -0.15A			-1.3	V
Input Capacitance	C_{ISS}	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz		25		pF
Output Capacitance	C_{OSS}			12		
Reverse Transfer Capacitance	C_{RSS}			5		
Turn-on Delay Time	$T_{D(ON)}$	V_{GS} = -4.5V, V_{DS} = -10V, R_L = 20Ω, R_G = 3Ω,		5		ns
Rise Time	T_r			4		
Turn-off Delay Time	$T_{D(OFF)}$			12		
Fall Time	T_f			7		

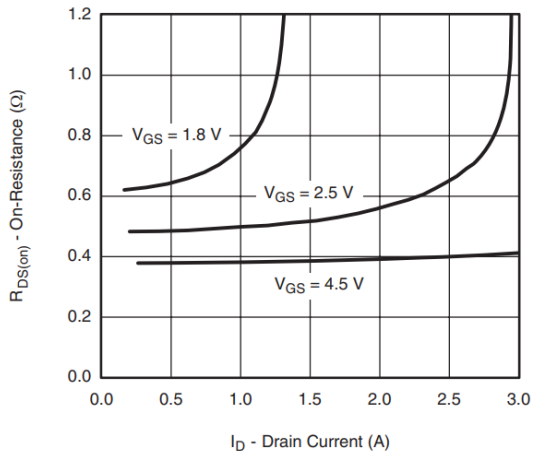
➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



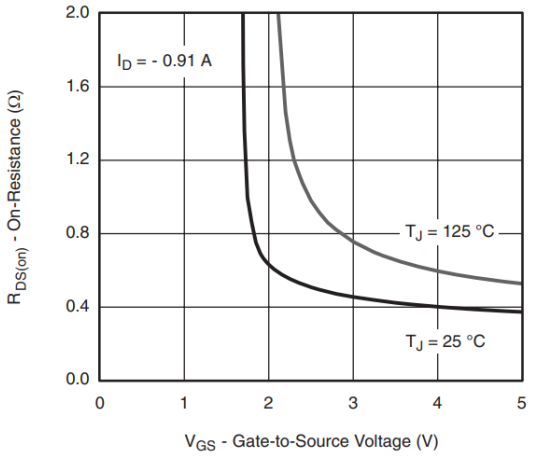
Output Characteristics



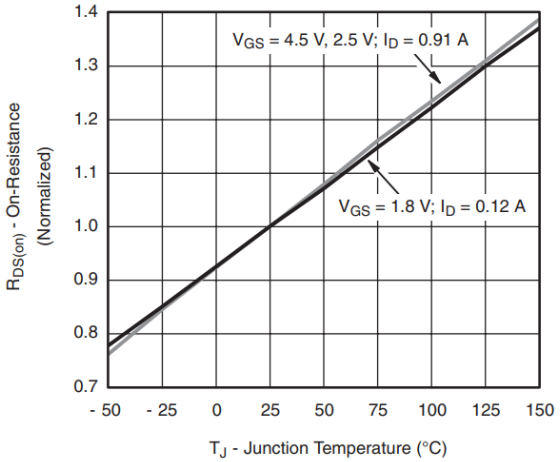
Transfer Characteristics



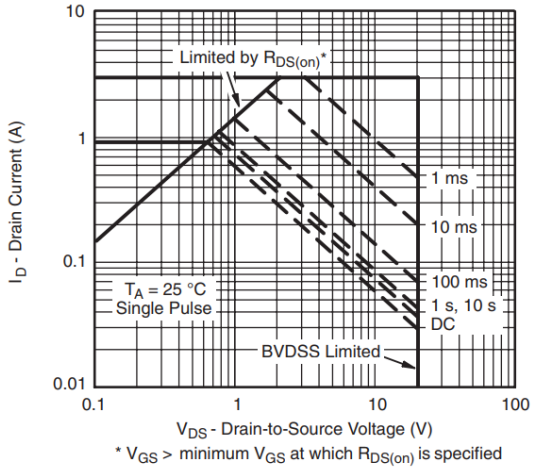
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage



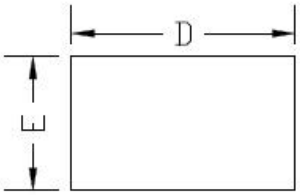
On-Resistance vs. Junction Temperature



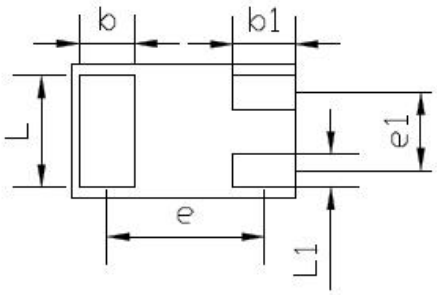
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

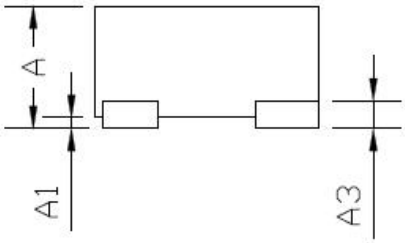
➢ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSION (MM)			
PKG	DFN1006		
REF.	MIN.	NOM.	MAX
A	>0.4	–	0.50
A1	0.00	–	0.05
A3	0.125REF.		
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b	0.20	0.25	0.30
b1	0.20	0.30	0.40
L	0.45	0.50	0.55
L1	0.10	0.15	0.20
e	0.675		
e1	0.35		

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